UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,019,342 B2
APPLICATION NO. : 10/719119
DATED : March 28, 2006
INVENTOR(S) : Douglas R. Hackler, Sr. et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1, line 38, ". . . inputs values . . ." change to --input values--

Column 1, line 39, ". . . output value of 0 . . ." change to --outputs a value of 0--

Column 1, line 49, ". . . overall architecture" change to --overall architecture.--

Column 2, line 18, ". . . gates result . . ." change to --gate result--

Column 2, line 21, ". . . bottom gates . . ." change to --bottom gate--

Column 3, line 1-2, ". . . device of FIG. 13 device after . . ." change to --device of FIG. 13 after--

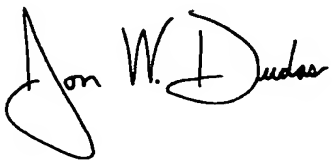
Column 7, line 46, ". . . to FIG. 12 to, a method . . ." change to --to FIG. 12, a method--

Column 7, line 60, ". . . the substrate layer 12 . . ." change to --the SOI layer 16--

Column 10, line 21, ". . .numerous complex circuit . . ." change to --numerous complex circuits--

Signed and Sealed this

Sixteenth Day of January, 2007



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